PULSE WIDTH MODULATION FOR CLASS D AUDIO POWER AMPLIFIER WITH 85% OF EFFICIENCY

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Abstract: In this paper a high efficiency PWM CMOS audio power amplifier is proposed. The original idea is based on the difference close-loop feedback technique and the difference pre-amp. Thus, we conceive a rail to rail comparator with a constant gm. This rail-to-rail PWM comparator with hysteresis architecture has been embedded in the audio power amplifier. The simulation results based on the TSMC 0.18µm CMOS process show that the power efficiency is 85%, the PSRR is ~70 dB, the power supply voltage range is 2.8–5.2 V, the THD+N in 1 kHz input frequency is 0.2%, the quiescent current is 2.7 mA. With the good performance, the audio power amplifier can be applied to various kinds of small and medium power audio amplification system such as DVD, LCD-TV, MP4 and wireless phones.

Key words: TSMC0.18um, Audio amplifier, PWM, CMOS, high efficiency, constant-gm, rail-to-rail comparator, difference.

1. INTRODUCTION:

Conventional class-A, B, or AB audio amplifiers directly amplify the analog signals and must work in the triode region. Although class-AB audio amplifiers have high fidelity, their power dissipation is obvious and conversion efficiency is below 50%, which hardly satisfy the requirement of energy saving. Some methods (such as employing push-pull output stage) are applied to compensate class-AB amplifiers. On the other hand, class-D amplifiers have many advantages over the class A, B, or AB mentioned above, the characteristic working on the switching state make the theoretic efficiency could be 100%, the practical value could be over 80%.

At present, class-D audio power amplifiers have already been used in consumer electronic products such as DVD, LCD-TV, MP4 and cell phone. Compared to the conventional class-AB audio power amplifier, its greatest advantage is the high efficiency, the practical efficiency would be over 80%, and the theoretical efficiency would be 100%. In the class-D audio power amplifier, we compare the audio signal and high frequency constant signal, then modulate this compared result using the constant frequency carrier waves, thus digital signal is converted into PWM signal, which is of changeable pulse width and constant carrier frequency (hundreds kHz generally). The PWM signal is amplified by MOSFET, and the amplified PWM signal carrier frequency is removed by LC low pass filter, thereby the original baseband audio signal drive speaker is obtained.

Based on the difference closed-loop feedback technique and the difference pre-amp, a high efficiency PWM CMOS class-D audio power amplifier is proposed, and a rail-to-rail comparator with window function is proposed as PWM comparator. The entire circuit is simulated and verified based on TSMC 0.18µm CMOS process, and is proved to be of high efficiency and low power consumption.

2. HIGH EFFICIENCY PWM CLASS-D AUDIO POWER AMPLIFIER

Since that system stability and noise characteristic of the closed loop system are much better than open loop system, we employ closed loop class-D audio power frequency architecture, with a feedback system, which is used to reduce the distortion. Considering the application without filter, full differential structure is used as input stage, a full differential operational amplifier cascaded as full differential integrator.

The proposed class-D amplifier as shown in Fig.1 is a fully differential amplifier with differential inputs and outputs. The fully differential amplifier consists of a differential amplifier and a common-mode amplifier. The differential amplifier ensures that the amplifier outputs a differential voltage on the output that is equal to the differential input times the gain.

Fig.1. Diagram of class-D audio power amplifier.

The common mode feedback ensures that the common mode voltage at the output is biased around
V_{DD}/2 regardless of the common-mode voltage at the input. The proposed class-D amplifier can still be used with a single-ended input. However, the proposed class-D amplifier should be used with differential inputs when in a noisy environment, like a wireless handset, to ensure maximum noise rejection.

The fully differential amplifier does not require a bypass capacitor. This is because any shift in the mid-supply affects both positive and negative channels equally and cancels at the differential output. GSM handsets save power by turning on and shutting off the RF transmitter at a rate of 225 Hz. The transmitted signal is picked-up on input and output traces. The fully differential amplifier cancels the signal much better than the typical audio amplifier. The diagram of class-D audio power amplifier in Fig.1 mainly includes input circuit, output drive circuit, feedback circuit, and so on. Input circuit is full differential operational amplifier, to limit the noise, increase the output voltage swing, and include the preceding proportional amplifier, connecting the full differential integrator constituted by full differential operational amplifier. PWM oscillator circuit generates a triangle wave, and the principle is to charge and discharge a capacity, the current for charging and discharging is equal, and so to form a triangle wave, the oscillating frequency of which is determined by the capacitance and current, 250 kHz in this paper. PWM module, the most significant configuration in class-D audio amplifier, is mainly composed with two hysteresis comparators, generates square waves with different duty cycle by comparison with full difference of the preceding input circuit. The feedback module adopting two parallel RC filters, and the signal is fed to the differential input terminal of full differential integrator through a full differential operational amplifier.

3. PRE-AMP AND FEEDBACK OF CLASS-D AUDIO POWER AMPLIFIER

Pre-amp and feedback of class-D audio power amplifier, full differential operational amplifier is applied as the input stage, to pre-amplify the input difference audio signal, and its single terminal gain is determined by the value of external connected resistance. For the best performance, the single terminal gain should set below 2, in that low gain could drive the chip to work on the best state, and the high input voltage may make the input terminal insensitive to the noise. Hence, when the input voltage is low, should be pre-amplified by an amplified circuit, instead of reducing the resistance to increase the circuit gain.

The first stage of the input configuration is full differential proportional amplifier, the second stage is full differential integrator. The feedback module adopting two parallel RC filters, and the signal is fed to the differential input end of full differential integrator through a full differential operational amplifier. So, the most significant configuration in class-D audio amplifier pre-amplifier and feedback segment is full differential CMOS operational amplifier.

![Fig.2 Full differential operational amplifier circuit.](image)

The full differential operational amplifier adopting the folded-Cascode configuration and the interior circuit is shown in Fig.2. The biased circuit and common-mode circuit is not presented due to the extent limit. M1–M2 compose the input stage difference amplifier, M3–M6 compose the output stage circuit, where M3, M4 are the power source, M5 and M6 are common-gate amplifier, M8 and M10 compose the active load transistor, M7 and M9 compose common-mode feedback circuit, M11 and M12 are clamping transistors used for reducing the operational amplifier setting time, having no effect on AC small signal characteristics. Analyzing the circuit in Fig.2 according to the small signal model, the voltage gain is

\[
A_v = \frac{g_m r_o \left( g_{mp} r_{up} \right)}{1 + r_{on} R_S + r_{off} R_N + r_{up} R_L}, \tag{1}
\]

where \( g_{mn}, r_{on}, g_{mp} \) and \( r_{up} \) are the transconductance and output resistance of NMOS and PMOS, respectively, and \( R_S, R_N \) are the limited output resistance of power supply. \( R_S \) is the source equivalent input resistance of NMOS, and \( R_N = 1/g_{mp}(1+R_L/r_{up}) \), so we can improve the limited output resistance of power supply to improve the DC gain of operational amplifier. If the output resistance of the load is much bigger than that of MOS, the max gain of full differential Cascode CMOS operational amplifier will be simplified as

\[
A_{v_{max}} = \frac{2g_m r_o \left( g_{mp} r_{up} \right)}{1}, \tag{2}
\]

Based on BSIM3V3 model of TSMC 0.1µm CMOS process, PWM comparator characteristic is simulated using SpectreS, under the condition that power voltage \( V_{DD} \) is 5 V, temperature is 27 °C (room temperature). The greatest open loop gain is 63 dB, phase margin is 62 °C, and unit gain band width frequency is 25 MHz, which can relax the class-D audio power amplifier.
requirement. The Power Supply Rejection Ratio PSRR is 68.6 dB, which can totally satisfy the wide power voltage application requirement of class-D audio power amplifier.

Fig.3. Rail-to-rail comparator with hysteresis function.

4. PWM RAIL-TO-RAIL COMPARATOR

In order to improve the accuracy and gain of the comparator, PWM comparator circuit employs two stage open loop comparator configuration, and for the reason that the comparator is applied in audio circuit, a noisy circumstance, also detect the signal variation at the threshold value, general comparators are inevitable to present noise at the output, thus we add the hysteresis configuration. M5, M13, M6, M10, M7, M11, and M8, M16 in Fig.3 are composed as corresponding hysteresis circuit, so to improve the anti-interference ability of comparator. As the comparator in class-D audio amplifier, its output modulation wave experienced a series digital logic change to control the power MOSFET. The best choice for the comparator common mode output to make MOSFET work normally is VSS – VDD; the full range output, which means it is necessary for the comparator common mode input range to be VSS – VDD, therefore, we must adopt rail-to-rail structure as the comparator input stage. This mentioned structure is usually made up of a parallel complementary P, N differential pair and the input stage configuration, composed of NMOS M3, M4 and PMOS M1, M2, is shown in Fig.3. The common mode input range for PMOS differential pair is $V_{SS} < V_{CM} < V_{DD} - |V_{GS} - |V_{DS}|$, $V_{SS} + V_{DS} + V_{GS} < V_{CM} < V_{DD}$ for NMOS pair, according to these two expressions, the common mode input range for this comparator is $V_{SS} < V_{CM} < V_{DD}$.

The common mode input range of Rail-to-Rail architecture could be divided into three working regions: When $V_{CM}$ is low, M1, M2 are turned on, M3, M4 are turned off, and the biased current is provided by $I_{bias1}$. When $V_{CM}$ is high, M3, M4 are turned on, M1, M2 are turned off, and the biased current is provided by $I_{bias2}$. If $V_{CM}$ is in intermediate range, the biased current is offered by both upper and lower tail currents, and then the sum of biased current will be $I_{bias1} + I_{bias2}$. The input stage total trans-conductance of rail-to-rail architecture is determined by:

$$I_D = \frac{1}{2} \mu C_{ox} \left( \frac{W}{L} \right) (V_{GS} - V_{TH})^2 \left( I + \lambda V_{DS} \right)$$  \hspace{1cm} (3)

Ignoring the channel modulation effect ($\lambda=0$), we get the total transconductance through derivation:

$$g_{m_{total}} = \mu_n \frac{W}{L} I_{bias2} + \mu_p \frac{W}{L} I_{bias1}$$  \hspace{1cm} (4)

According to Eq.(4), rail-to-rail circuit regulates the input stage total biased current to realize the total transconductance to be constant, the comparator performance improved. The comparator output stage adopts the basic difference structure without constant-current source, shown in Fig.3. M19, M20 are the differential input, M18, M17 compose the image load, M20, M17 are the typical class-AB output architecture, and therefore realizing rail-to-rail voltage output. At the same time, every MOS in output stage is chosen as $(W/L)_{17} = (W/L)_{18} = (W/L)_{20} = 3\mu m/1\mu m$, which means they are matching with each other, and do the small signal analysis to get the gain expression as

$$A_V = g_{m19,20} \left( r_{o19,20} \right) \left( r_{o17,18} \right)$$  \hspace{1cm} (5)
Based on BSIM3V3 model of TSMC 0.18 µm CMOS process, PWM comparator characteristic is simulated using SpectreS, under the condition that power voltage $V_{DD}$ is 5 V, temperature is 25 °C (room temperature). Analyzing the circuit with AC Analysis, the simulated results are shown in Fig.4. The comparator DC gain shown in Fig.4, is 51 dB and PSRR is 58 dB.

The rise and fall transfer time delay of the comparator is 44 and 5 ns respectively. Analyzing the circuit and the total time delay is 24.5 ns. The comparator positive slew rate and negative slew rate is 360 and –360 V/µs respectively. The simulated result suggests that rise delay is longer than fall delay. Because of the reason that M17 and M20 in the output stage have the same $W/L$ and the different mobility between holes in PMOS and electrons in NMOS leading to the different driving ability between these two kinds of transistors. The designed comparator is mainly applied in audio, working under low frequency state, 250 kHz. On the basis of the simulated results, we can conclude that, when the frequency is low the comparator is of shorter transfer delay, the quicker response. The simulated dc characteristic, and ICMR range is from 0 to 5 V, at the same time output swing reaches the full range. Hence, output signal of the comparator can thoroughly drive the following audio logic circuit, and thereby ensure the fidelity of the audio signals.

The comparator waveform, at normal state, with sine wave (frequency 10 kHz and amplitude in the range of 1.3–3.7 V) and triangle wave (frequency 250 kHz and amplitude in the range of 1.2–3.8 V) as the input waves, is shown in Fig.5, and the imaginary line is the sampled PWM wave. To avoid the signal distortion after sampling, the amplitude of sine wave should be lower than that of triangle wave, and we regulate the gain of preamplifier to avoid over regulation for the large amplitude signals.

Based on TSMC 0.18 µm N-well CMOS process, the proposed high efficiency class-D audio power amplifier is simulated, silicon verified and measured. When the load is the equivalent loudspeaker 8 Ω, $V_{DD}$ = 3.6V, input signal is 10 kHz 300 mV differential sine wave, the simulated results of class-D audio power amplifier in the 0.18µm CMOS, the stabilized output sine wave signal is complete, THD+N is 0.2%. When the output power is reach to 2.5 W, the conversion efficiency is about 85%. The power supply is in the range of 2.5–5.5 V, PSRR is about –70 dB.

6. CONCLUSION

This paper proposed a high efficiency PMOS CMOS class-D audio power amplifier based on feedback close loop configuration, adopting full differential pre-amp and full differential feedback, and proposes a rail-to-rail comparator with hysteresis architecture as the PWM comparator. The entire circuit is simulated, verified and measured based on TSMC 0.18 µm CMOS process. The maximum conversion efficiency is up to 90%, the range of power supply is 2.5–5.5 V, and THD is less than 1% with 10 kHz frequency; for good performance this amplifier can be used in various kinds of small and medium power audio amplification system.

7. REFERENCES