VHDL-AMS modeling and simulation of a direct sequence spread spectrum (DS-SS) transmitter

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Abstract—Many recent standards in telecommunications field are based on CDMA spread spectrum transmissions. In this paper, we describe a methodology for top-down design, modeling, and simulation of CDMA transmitter system using hardware description language VHDL-AMS. Details of VHDL-AMS implementation for each elementary block are shown. This paper together with the developed library of CDMA transmitter blocks are targeted towards engineers who work on behavioral modeling and simulation of complete CDMA systems using hardware description languages.

Index Terms—CDMA, Wireless DS-SS transmitter; VHDL-AMS language; FPGA implementation

I. INTRODUCTION

Code division multiple access CDMA is a channel access method used by various radio communication systems, it is the backbone of the third-generation mobile telecommunications standard UMTS and WiMAX in deployment nowadays [1]. This technique is used for a variety of reasons, including the establishment of secure communications, increasing resistance against interference and jamming, to prevent detection, and to limit power flux density. A code is assigned for each transmitter, this allows several users to be multiplexed over a single communication channel, and send information simultaneously. The frequency reuse limitations, as in FDMA and TDMA, are less in CDMA which makes it an attractive technique to GSM.

CDMA codes are designed to have very low cross-correlation to improve the bandwidth efficiency of cellular CDMA systems [2]. And allow a capacity improvement of the communication system and thus a better management of the available resources.

In a CDMA transmitting-receiving system, the principal parts which define the communication performances are code sequences, their lengths and synchronization between the reception and the emission. A good synchronization and a large spreading length reduce enormously the multiple access interference (MAI).
On the other side, the concept of time to market became an important constraint during a new product design. The goal is to be able to reduce the gap between a linear productivity and an exponential growth of circuit complexity. The use of flexible and reusable prototypes allows to make reliable and to decrease the design cycle.

A popular approach to modeling and simulation of complex mixed-signal (digital/analog/RF) systems is behavioral modeling, which is more time efficient than full circuit-level simulation and is invaluable for verification purposes. Behavioral modeling in modern electronic design flow is commonly performed with high-level hardware description languages (HDLs) [3]. Two most often used HDLs are VHDL-AMS [4] (an IEEE standard) and Verilog-A.

This work enters in this context, indeed in a first part, we present a digital-analog circuits description, behavioral modeling and simulation of CDMA communication system emission part as well in baseband as in radio frequency (RF). The length of the spreading codes is flexible. We present our library of simple blocks (digital/RF) that can be run in any HDL simulator with proper language support functionality. Any additional level of detail can be further added to these blocks, down to the circuit level inclusively.

II. SYSTEM PRESENTATION

The system to develop is based on the 802.11 standard, making it possible to transmit in the waveband of width 80 MHz centered to 2.44GHz and uses a phase numerical modulation DBPSK (Differential Binary Phase Keying Shift) [5]. The synoptic diagram of the transmitter is shown in Fig 1. The transmitter includes the numerical stages carrying out the signals coding to be transmitted and the spectrum spreading function via a pseudo-random sequence. The RF part emits the spread out signal at carrier frequency of 2.44 GHz.

III. TRANSMITTER VHDL-AMS MODELING

The synoptic deduced from the functional diagram in VHDL-AMS is shown in Fig 2.

Fig 1: Transmitter model block diagram.

Fig 2: Transmitter coding synoptic

For each block we wrote the associated model in VHDL using simulator MODELSIM (digital) and SIMPLORER (AMS). Then, the models are validated by the observation of the principal signals

III.2. Baseband part modeling

The digital Transmitter part architecture is presented in Fig. 3:

Fig 3: Transmitter baseband part block diagram

It consists of 3 blocks: the differential coder, the spreading code generator and the multiplier.

The differential coding function is used to avoid a coherent detection in the demodulation process by the receiver and provides an unambiguous signal reception. This block is carried out using two logic gates (NOT) and (XOR).
a. PN Code generator

The spreading sequences used for the CDMA must be chosen to respect the orthogonality condition. To achieve this condition, specifically we can use the maximal length sequence or the \( m \)-sequence, so named because its sequences are of maximal length, often referred as pseudo-noise (PN) codes. \( M \)-Sequences have good auto-correlation properties and have been used in many applications including the IS-95 standard. An \( m \)-sequence can be easily generated by using a shift register with the help of a simple feedback logic according to a particular primitive polynomial. Therefore, the \( m \)-sequence could be considered as a CDMA code set that can be generated with the least hardware complexity.

As presented in Fig 4, for a \( n \)-length linear feedback shift register (LFSR), the PN-Code generation requires a polynomial \( i(n) \) for initialization, and a primitive generator polynomial \( pg(n) \). The \( m \)-Sequences can be generated from output of the LFSR with certain feedback logic.

![Fig 4: Exemple of Galois implementation of a LFSR for m-sequence generation](image)

The generator polynomial governs all major characteristics of the generator. For a given generator polynomial, there are two ways [6] of implementing LFSR. A Galois feedback generator uses only the output bit to add (in Galois field) several stages of the shift register and is desirable for high-speed hardware implementation as well as software implementation. The other way, known as a Fibonacci feedback generator, can generate several delays of sequences without any additional logic.

A \( n \)-length LFSR gives a \( m \)-sequence length of \( N=2^n-1 \). In our work, for the implementation we use a 12-LFSR, it can thus generate codes with a maximum length \( N=4095 \) and lead to higher process gain in a noisy environment.

As an example, for a 12-LFSR, we obtain different lengths of PN-code (7, 15, 31, 63…) by modifying the \( pg(12) \) coefficients.

<table>
<thead>
<tr>
<th>( N )</th>
<th>( pg )</th>
<th>PN-code</th>
</tr>
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<tbody>
<tr>
<td>7</td>
<td>000000000101</td>
<td>1110100</td>
</tr>
<tr>
<td>15</td>
<td>00000001001</td>
<td>111101011001000</td>
</tr>
<tr>
<td>31</td>
<td>00000010010</td>
<td>1010111011000111110011010010000</td>
</tr>
</tbody>
</table>

Table: Generated PN codes for different \( pg (12) \) coefficients

b. Transmitter parts association

To associate the transmitter parts, time synchronization between data and \( m \)-sequence is essential. To ensure this constraint, a single master clock generator is used as reference clock for the entire system. The orthogonal code generators should operate at master clock rate and the data source should operate at \( N \) fraction of master clock rate, where \( N \) is the length of orthogonal code (Fig 5). The flow chart of the synchronized parts of the transmitter are presented in Fig 6.

![Fig 5: Transmitter system block diagram](image)

At the digital part end, the multiplication between the differential encoded data and the spreading code is achieved by exclusive-ORing the data with the spreading code (logical XOR operation).
All the parts of the transmitter system were implemented completely using VHDL. After association of all these blocks, the simulation results are presented in Fig 7.

The figure shows The PN generator output for initializing code 011(5). The PN-code 1110010 and the spread out data can be seen aligned with the seven master clock cycles.

**III.2. Radiofrequency part modeling**

The radiofrequency stages modeling of the transmitter takes advantage of analog and mixed functionalities of VHDL-AMS language. These stages consist on multipliers, oscillators carrying out the BPSK modulation on a carrier frequency, band-pass filters and a low-pass filter in order to eliminate double frequencies at the demodulator output.

BPSK modulation consists of a carrier phase shift according to the binary data transmitted [8]. This is done by the implementation of a digital-analog multiplier: a mix of binary signal (data_etalee) and the carrier frequency (2,44GHz). This function is described in the following flow chart (fig 7):

The results show that each change of data state corresponds to a carrier frequency phase shift of π (rad).

**IV. CONCLUSION**

In this paper, we described a methodology for modeling and simulation of complete CDMA transmitter (RF and base-band parts) using VHDL-AMS. We presented and implemented all the blocks constituting the system (differential coding, PN-Code generation, spreading spectrum and modulation). The length of the generated codes can easily be modified by changing sole the input coefficients of the polynomial generator without modification of the implemented system. Simulations tests and the signals obtained validate the descriptions suggested for the parameters presented in the specifications (standard 802.11). This model can be considered as a new IP and can
be reused easily by many teams. We will propose an architecture of this transmitter for an implementation on an FPGA. We project to carry out the receiver offering a good synchronization with our transmitter. We hope that this paper will help VHDL-AMS designers to better understand the process of HDL modeling and simulation for CDMA transceiver.

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